Amendments to the Claims

1. (CURRENTLY AMENDED)   Apparatus (80) comprising an input stage (50; 61) with - an NMOS transistor doublet (N1, N2) having a first differential input (52.1, 53.1; 62.1, 63.1) for receiving input signals, - a PMOS transistor doublet (P3, P4) having a second differential input (52.2, 53.2; 62.2, 63.2) for receiving input signals, and - switching means for receiving and selectively directing analog input signals either to said first differential input (52.1, 53.1; 62.1, 63.1) or to said second differential input (52.2, 53.2; 62.2, 63.2), said means being controlled by a switching signal (Φ, Φ̄), whereby the ratio of the transconductance of the NMOS transistor doublet (N1, N2) and the transconductance of the PMOS transistor doublet (P3, P4) is kept constant.

2. (CURRENTLY AMENDED)   The apparatus (80) of claim 1, wherein the switching means direct the input signals to said first differential input (52.1, 53.1; 62.1, 63.1) if the input signals have positive gamma data and to said second differential input (52.2, 53.2; 62.2, 63.2) if the input signals have negative gamma data.

3. (CURRENTLY AMENDED)   The apparatus of claim 1 or 2 claim 1, wherein - the NMOS transistor doublet (N1, N2) comprises two NMOS transistors, each having a gate, whereby the gate of the first of the two NMOS transistors is connectable to a first input node (IN+) and the gate of the second of the two NMOS transistors is connectable to a second input node (IN-), - the PMOS transistor doublet (P3, P4) comprises two PMOS transistors, each having a gate, whereby the gate of the first of the two PMOS transistors is connectable to the first input node (IN+) and the gate of the second of the two PMOS transistors is connectable to the second input node (IN-).

4. (CURRENTLY A MENDED)   The apparatus of claim 3,
wherein - the gate of the first of the two NMOS transistors is connectable to a first reference node (66.1) being biased with a first reference voltage (HIGH_REF), and the gate of the second of the two NMOS transistors is connectable to the first reference node (66.1) being biased with a second reference voltage (LOW_HIGH), - the gate of the first of the two PMOS transistors is connectable to a second reference node (66.2) being biased with a second reference voltage (HIGH_LOW) and the gate of the second of the two PMOS transistors is connectable to the second reference node (66.2).

5. (CURRENTLY AMENDED)   The apparatus of claim 1, wherein the input stage (50; 61) is a rail-to-rail input stage.

6. (CURRENTLY AMENDED)   The apparatus of claim 1, wherein the switching means comprise a plurality of switches ~~(S1 through S8)~~ in order to selectively direct the input signals to said first differential input ~~(52.1, 53.1; 62.1, 63.1)~~ or said second differential input ~~(52.2, 53.2; 62.2, 63.2)~~.

7.(CURRENTLY AMENDED)   The apparatus of ~~claim 1 or 2~~claim 1, wherein said switching signal ~~(Φ, Φ̄)~~ is a digital switching signal.

8.(CURRENTLY AMENDED)   The apparatus according to ~~one of the claim 1 through 4~~claim 1, wherein transistors serve as switches ~~(S1 through S8)~~.

9.(CURRENTLY AMENDED)   The apparatus of ~~claim 1 or 2,~~ claim 1 wherein the NMOS transistor doublet ~~(N1, N2)~~ and the PMOS transistor doublet ~~(P3, P4)~~ are part of a folded cascode rail-to-rail input stage ~~(61)~~ and wherein the folded cascode rail-to-rail input stage ~~(61)~~ is connected to a second stage ~~(64)~~ comprising a rail-to-rail output stage amplifier.

10. (CURRENTLY AMENDED)   Apparatus comprising a source driver bank ~~(80)~~ with a plurality of apparatus according to ~~one of the previous claims~~claim 1, and further comprising a bus ~~(43; 91)~~ for receiving input signals.

11. (CURRENTLY AMENDED)   The apparatus of claim 10, further comprising a gate driver bank ~~(45)~~ and an LCD panel ~~(46)~~.

12. (CURRENTLY AMENDED)   The apparatus of ~~claim 10 or 11~~claim 10, further comprising a control signal generator ~~(90)~~ for generating the switching signal ~~(Φ, Φ̄)~~.

13. (CURRENTLY AMENDED)   The apparatus of ~~claim 10, 11 or 12~~ claim 10 being part of a panel module ~~(40)~~.